WHAT IS CLAIMED IS:

1. A multi-port instruction/data integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and which stores a part of instructions and data stored in the main memory, comprising:

a plurality of banks; and

a plurality of ports including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor, and a data port unit consisting of at least one data port used to access data from the parallel processor,

wherein a data width which can be specified to the bank from the instruction port is set larger than a data width which can be specified to the bank from the data port.

2. The multi-port instruction/data integrated cache according to claim 1, wherein a plurality of non-continuous banks can be accessed from the instruction port, and

all the banks can be accessed from the data port.

3. The multi-port instruction/data integrated cache according to claim 1 or 2, wherein the multi-port instruction/data integrated cache is constituted by an HMA structure.

4. The multi-port instruction/data integrated

cache according to claim 1 or 2, wherein the multi-port instruction/data integrated cache is constituted by a crossbar switch network structure.

5. A multi-port instruction/trace integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and in which an instruction cache and a trace cache are integrated, comprising:

a multi-port bank memory which has a plurality of banks which store a part of instruction data stored in the main memory and a plurality of ports;

instruction data reading means for reading specified instruction data as instruction data of the instruction cache from the multi-port bank memory when the parallel processor accesses the multi-port bank memory as the instruction cache; and

trace data reading means for reading specified instruction data as trace data of the trace cache from the multi-port bank memory when the parallel processor accesses the multi-port bank memory as the trace cache.

6. A multi-port instruction/trace integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and in which an instruction cache and a trace cache are integrated, comprising:

a multi-port bank memory which has a plurality of banks which store a part of instruction data stored in

the main memory and a plurality of ports;

a tag directory which has a plurality of areas each corresponding to an index set to a middle-order digit in a fetch address outputted from the parallel processor, each of the areas storing therein an identification bit indicating whether instruction data to be accessed is data of the trace cache, a tag 1 set to a high-order digit in the fetch address, a tag 2 set to a lower-order digit in the fetch address, and a plurality of addresses which specify instruction data stored in each bank of the multi-port bank memory;

an instruction cache hit judgment circuit which judges that the instruction data to be accessed is stored in the multi-port bank memory based on the tag 1 and the identification bit;

a trace cache hit judgment circuit which judges that an instruction data string to be accessed is stored in the multi-port bank memory based on the tag 1, the tag 2 and the identification bit; and

a fetch address selector which selects a predetermined number of addresses among a plurality of addresses stored in a corresponding area of the tag directory in accordance with a hit judgment by the trace cache hit judgment circuit, supplies them to the multi-port bank memory, and causes instruction data in each bank to be simultaneously read.

7. A multi-port instruction/trace integrated

cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and in which an instruction cache and a trace cache are integrated, comprising:

a multi-port bank memory which has a plurality of banks which store a part of instruction data stored in the main memory and a plurality of ports;

a plurality of tag directories to which fetch addresses which are based on a fetch address of the parallel processor and different from each other are inputted from a fetched line address cache, and each of which has a plurality of areas each corresponding to an index set to a middle-order digit in the inputted fetch address, each of the areas storing an identification bit indicating whether instruction data to be accessed is data of the trace cache, a tag 1 set to a higher-order digit in the fetch address, and a tag 2 set to a lower-order digit in the fetch address;

a plurality of instruction cache hit judgment circuits which are provided in accordance with the respective tag directories and judge that the instruction data to be accessed is stored in the multi-port bank memory based on the tag 1 and the identification bit;

a plurality of trace cache hit judgment circuits which are provided in accordance with the respective tag directories and judge that an instruction string to

be accessed is stored in the multi-port bank memory based on the tag 1, the tag 2 and the identification bit; and

a bank access circuit which supplies each fetch address inputted to a corresponding tag directory to the multi-port bank memory in accordance with a hit judgment by the respective cache hit judgment circuits, and simultaneously reads instruction data of each bank.

8. A multi-port instruction/trace integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and in which an instruction cache and a trace cache are integrated, comprising:

a multi-port bank memory which has a plurality of banks which store a part of instruction data stored in the main memory and a plurality of ports;

an instruction tag directory having a plurality of areas each of which corresponds to an index set to a middle-order digit in a fetch address outputted from the parallel processor, each of the areas storing a tag 1 set to a higher-order digit in the fetch address;

a trace tag directory having a plurality of areas each of which corresponds to an index set to a middle-order digit in a fetch address outputted from the parallel processor, each of the areas storing a tag 1 set to a higher-order digit in the fetch address, a tag 2 set to a lower-order digit in the fetch address, and

a plurality of addresses each of which specifies instruction data stored in each bank of the multi-port bank memory;

an instruction cache hit judgment circuit which judges that instruction data to be accessed is stored in the multi-port bank memory based on the tag 1;

a trace cache hit judgment circuit which judges that an instruction data string to be accessed is stored in the multi-port bank memory based on the tag 1 and the tag 2; and

a fetch address selector which selects a predetermined number of addresses among a plurality of addresses stored in a corresponding area of the tag directory in accordance with a hit judgment by the trace cache hit judgment circuit, supplies them to the multi-port bank memory, and causes instruction data in each bank to be simultaneously read.

9. A multi-port instruction/trace integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and in which an instruction cache and a trace cache are integrated, comprising:

a multi-port bank memory having a plurality of banks which store a part of instruction data stored in the main memory and a plurality of ports;

a plurality of instruction tag directories to which fetch addresses which are based on a fetch

address of the parallel processor and different from each other are inputted from a fetched line address cache, and each of which has a plurality of areas each corresponding to an index set to a middle-order digit in the inputted fetch address, each of the areas storing a tag 1 set to a higher-order digit in the fetch address;

a plurality of trace tag directories to which fetch addresses which are based on the fetch address of the parallel processor and different from each other are inputted from the fetched line address cache, and each of which has a plurality of areas each corresponding to an index set to a middle-order digit of the inputted fetch address, each of the areas storing a tag 1 set to a higher-order digit in the fetch address, and a tag 2 set to a lower-order digit in the fetch address;

a plurality of instruction cache hit judgment circuits which are provided in accordance with the respective instruction tag directories, and judge that instruction data to be accessed is stored in the multi-port bank memory based on the tag 1;

a plurality of trace cache hit judgment circuits which are provided in accordance with the respective instruction tag directories, and judge that an instruction data string to be accessed is stored in the multi-port bank memory based on the tag 1 and the tag

2; and

a bank access circuit which supplies each fetch address inputted to a corresponding tag directory to the multi-port bank memory in accordance with a hit judgment by each of the cache hit judgment circuits, and simultaneously reads instruction data in each bank.

10. The multi-port instruction/trace integrated cache according to claim 6 or 8, wherein a plurality of addresses stored in each area of the tag directory are updated based on an address of each instruction executed when a corresponding area is hit on the last occasion.

11. The multi-port instruction/trace integrated cache according to claim 10, wherein a plurality of addresses stored in the respective areas of the tag directory include an address of each instruction executed when the corresponding area is hit on the last occasion and an address of a branch target instruction that branching is possible after the aforesaid instruction.

12. The multi-port instruction/trace integrated cache according to claim 10, wherein the fetch address selector selects the predetermined number of addresses based on a branch prediction of each instruction inputted from a branch predictor.

13. The multi-port instruction/trace integrated cache according to claim 11, wherein the fetch address

selector selects the predetermined number of addresses based on a branch prediction of each instruction inputted from a branch predictor.

14. The multi-port instruction/trace integrated cache according to claim 7 or 9, wherein a plurality of the fetch addresses outputted from the fetched line address cache are updated based on an address of each instruction executed when the fetch addresses are hit on the last occasion.

15. The multi-port instruction/trace integrated cache according to claim 14, wherein a plurality of the fetch addresses outputted from the fetched line address cache include an address of each instruction executed when the fetch addresses are hit on the last occasion and an address of a branch target instruction that branching is possible after the aforesaid instruction.

16. A multi-port instruction/trace/data integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory, and which stores a part of instructions, traces and data stored in the main memory, comprising:

a plurality of banks; and

a plurality of ports including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor, a trace port unit consisting of at least one trace port

used to access a trace from the parallel processor, and a data port unit consisting of at least one data port used to access data from the parallel processor,

wherein each data width which can be specified to the bank from the instruction port and the trace port is set larger than a data width which can be specified to the bank from the data port.

17. A multi-port instruction/trace/data integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and in which an instruction cache, a trace cache and a data cache are integrated, comprising:

a multi-port bank memory which has a plurality of banks which store a part of instructions and data stored in the main memory, and a plurality of ports;

a tag directory having a plurality of areas each corresponding to an index set to a middle-order digit in a fetch address outputted from the parallel processor, each of the areas storing an identification bit indicating whether an instruction or data to be accessed is data of the trace cache, a tag 1 set to a higher-order digit in the fetch address, a tag 2 set to a lower-order digit in the fetch address, and a plurality of addresses which specify an instruction or data stored in each bank of the multi-port bank memory;

an instruction cache hit judgment circuit which

judges that the instruction or data to be accessed is stored in the multi-port bank memory based on the tag 1 and the identification bit;

a trace cache hit judgment circuit which judges that the instruction to be accessed is stored in the multi-port bank memory based on the tag 1, the tag 2 and the identification bit;

a fetch address selector which selects a predetermined number of addresses among a plurality of addresses stored in a corresponding area of the tag directory in accordance with a hit judgment by each cache hit judgment circuit, supplies them to the multi-port bank memory, and causes instructions or data in each bank to be simultaneously read; and

a selection circuit which selects data required by the parallel processor from a plurality of sets of data read from the multi-port bank memory.